**ECE 385**

Fall 2021

Experiment #1

**Introductory Experiment**

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Section AB6, N/A

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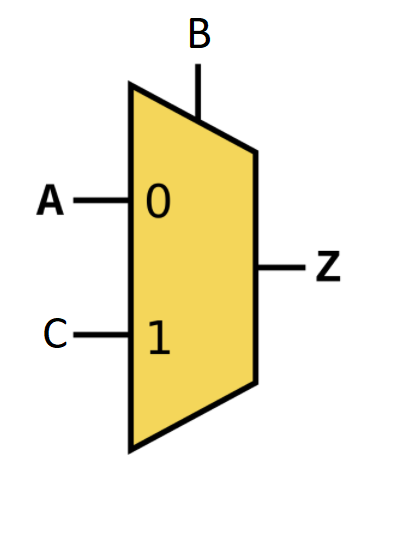
**Purpose:**

The purpose of this lab was to introduce the lab equipment and software that will be used in ECE 385. The content of the lab is about designing debugging a 2:1 multiplexer circuit by adding a redundant component of a k-map to mitigate the static-1 hazard. This would be useful to keep in mind to ensure any CMOS circuit works properly.

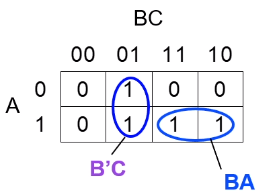
**Written Description of Circuit**

The circuit serves the purpose of a 2:1 Multiplexer, selecting between two input signals A and C with a third controlling signal B to output a signal Z.

**High Level Block Diagram**



Designing this mux circuit was accomplished using the following truth table and k-map, provided by the lab1 walkthrough:

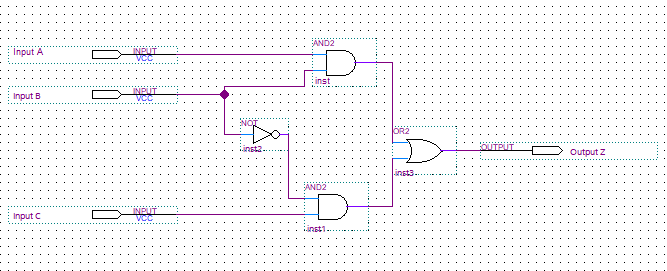


The truth table is then used to create a Boolean expression in minimal SOP form for both the static hazard variant and the fixed variant later on.

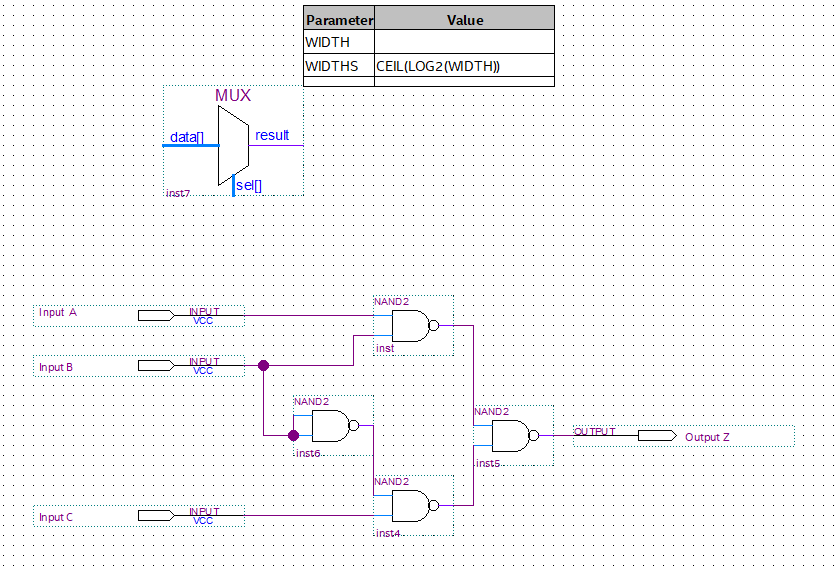


Then the Boolean expressions are used to make a logic diagram, which is then converted into a NAND only logic diagram (replacing NOT gates with a combined input NAND, AND gates with NANDs and then using DeMorgan’s laws to convert the OR gate with inverted inputs to a NAND gate), so that it may be compatible for a schematic for the SN7400 chip(s) as it has quad NANDs.

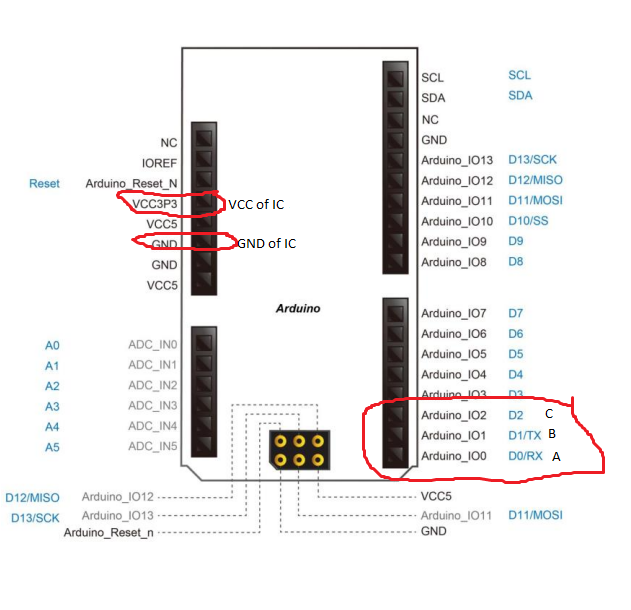
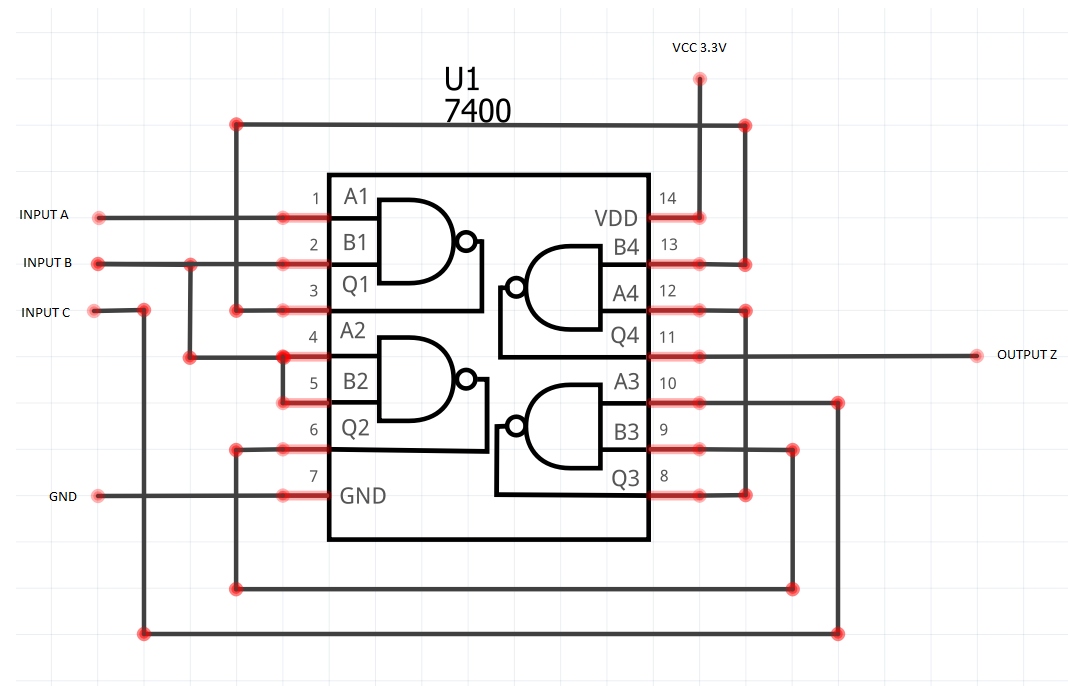
Simple logic diagram:



NAND-specific logic diagram:

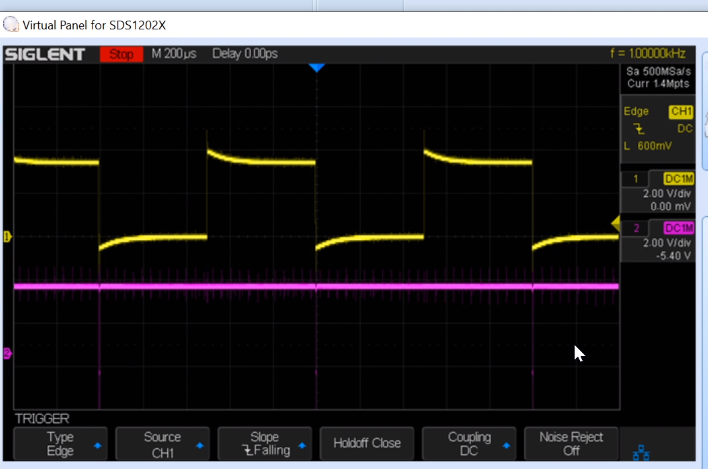


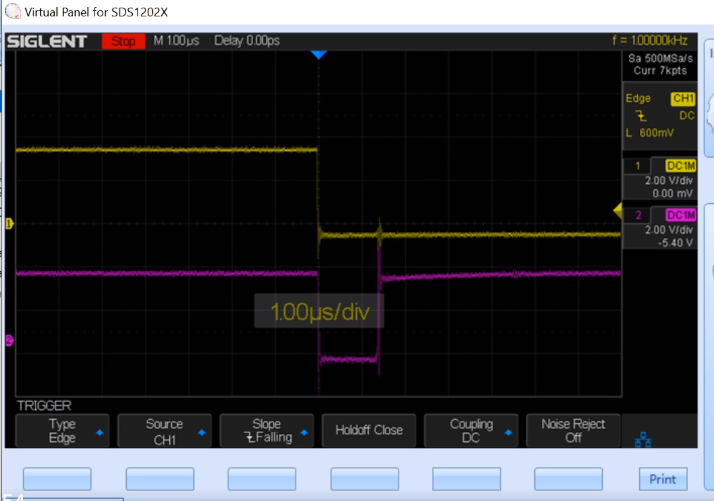
In the schematic, the FPGA board will be used as a switchbox for the inputs of the multiplexer and the LED strip brick will be used as the output to indicate high or low. To use the chip(s) together with the FPGA board, the IC’s logic gates are powered by attaching the VCC pin to the 3.3V pin of the FPGA and the GND pin to the ground pin on the FPGA.



Then Quartus is used to flash the bitstream of the virtual switchbox onto the FPGA, and the inputs A, B, and C are connected to the Arduino pins 0, 1, & 2, respectfully, where A and C are the two inputs and B is the selecting input. With the output Z of the IC being connected to the LED with a resistor in series to ground, the circuit will seem to function as intended. However, upon further investigation, using a 1 KHz clock as an input to the selector input B, a noticeable glitch is present when zooming in with an oscilloscope. When switching between the two inputs even while both high, a sudden and short drop off in voltage is visible in a very narrow time frame of ~1 microsecond, as a result of the uncovered (yet redundant) minterm in the initial truth table.

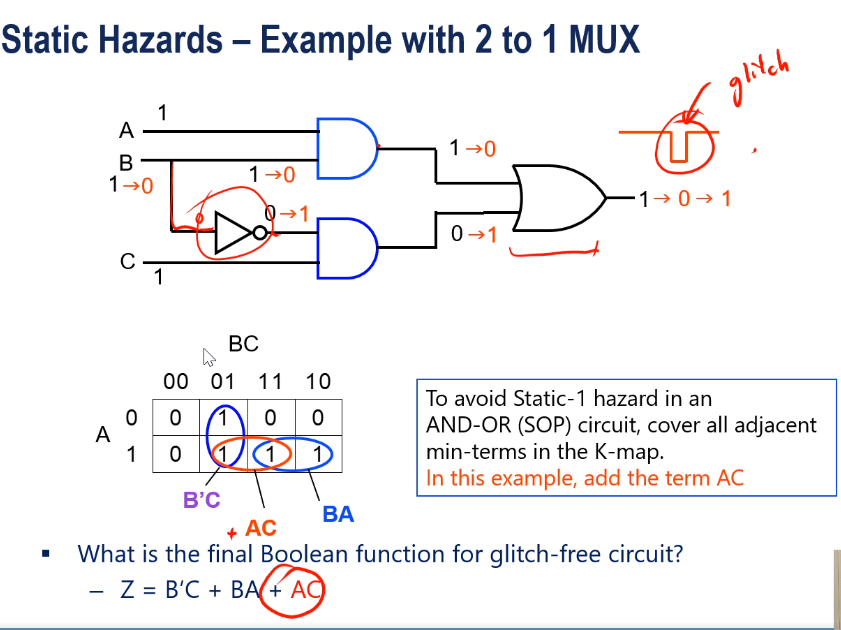
Yellow channel: 1KHz clock

Pink channel: output signal Z 

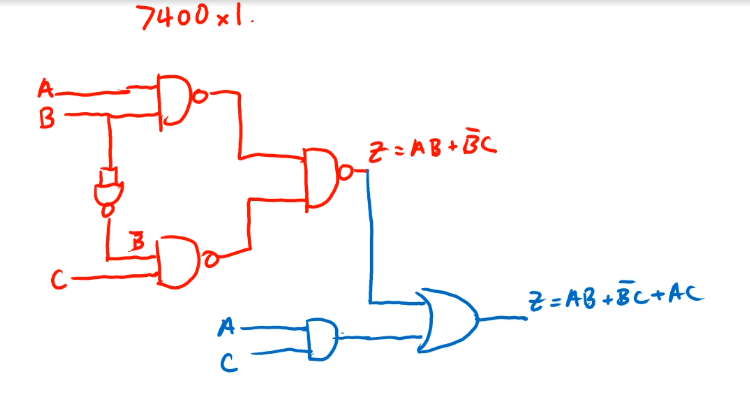


In order to fix this issue, the redundant minterm of the truth table is included and the boolean expression is changed correspondingly. In this case an additional term AC is added. (K-map and truth table provided by lab1 walkthrough below).

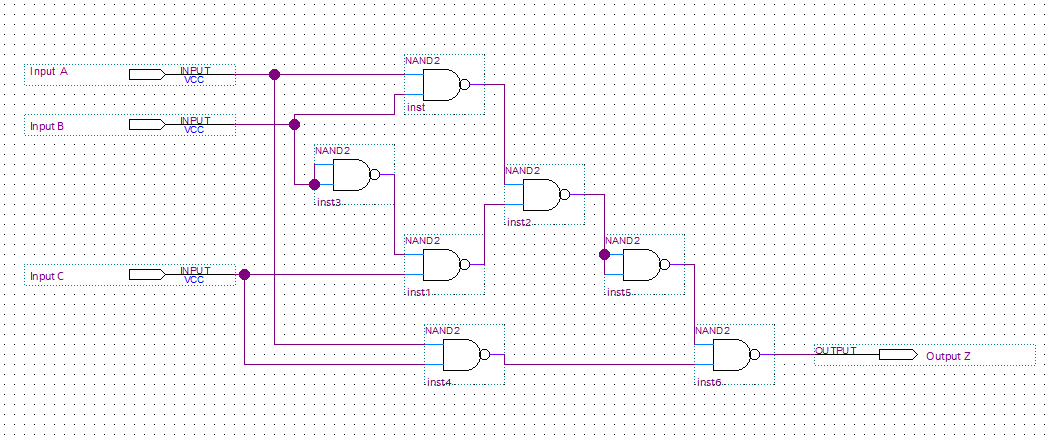
Diagram

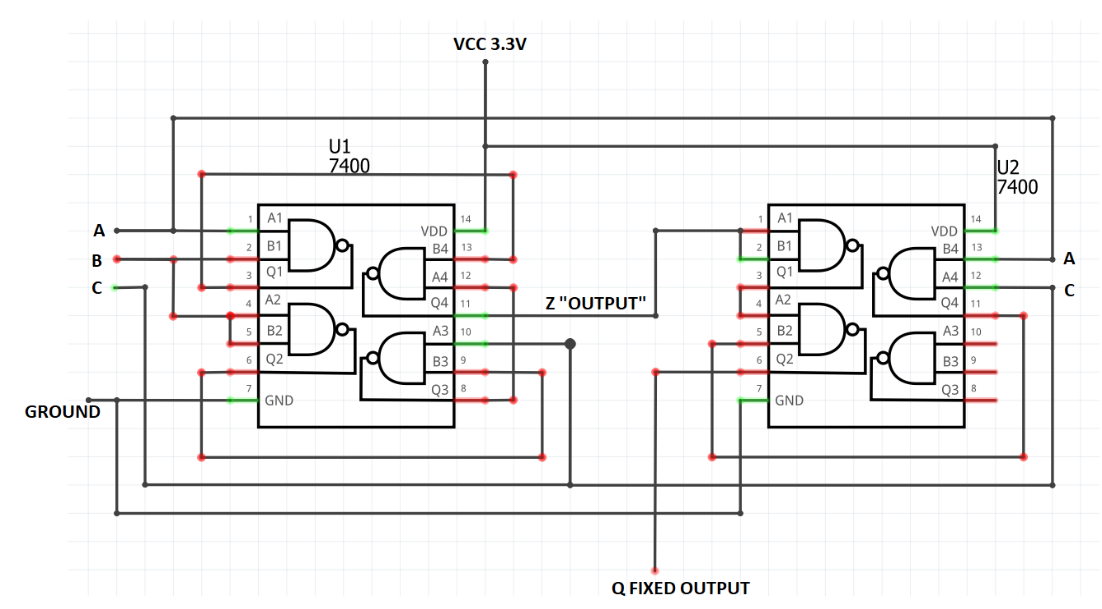
Description automatically generatednew boolean expression:

Consequently, an adjustment to the boolean expression will constitute a change to the logic diagram. A basic change would be to add an AND gate and an OR gate in the following order:

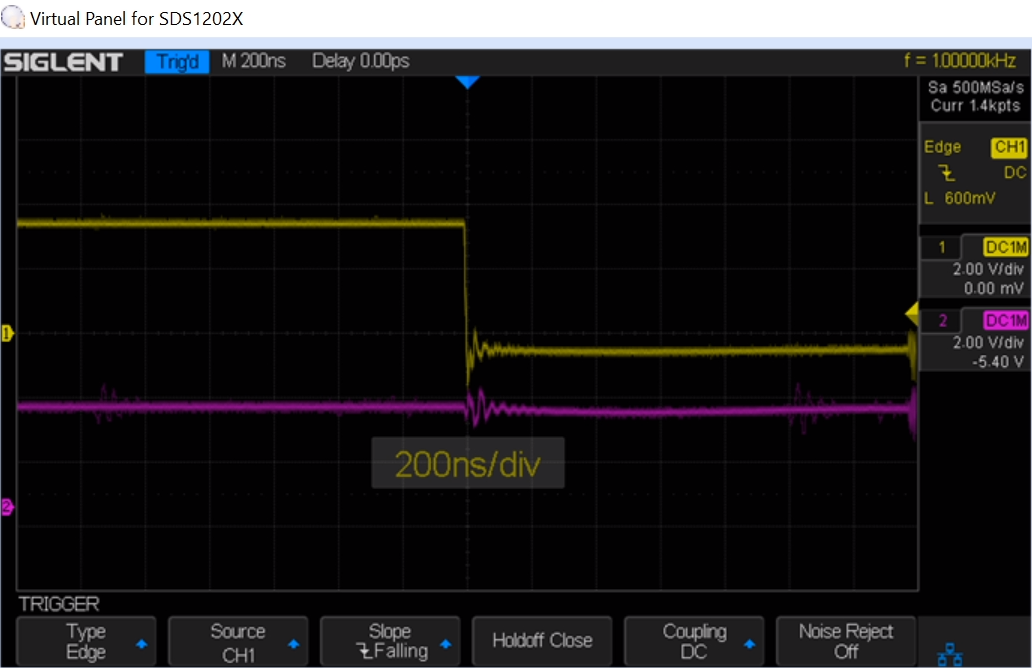
(as shown in the lab1 walkthrough)

To continue working with the 7400 chips, this logic diagram can be converted into a NAND-only logic diagram by simply swapping out the AND gate with a NAND, inverting the output of the previous logic diagram with a NAND (functioning as a NOT), and replacing the OR gate with a NAND because of DeMorgan’s law. Adding in these extra NAND gates will require a total of two 7400-chips since a total of 7 NANDs are at work.

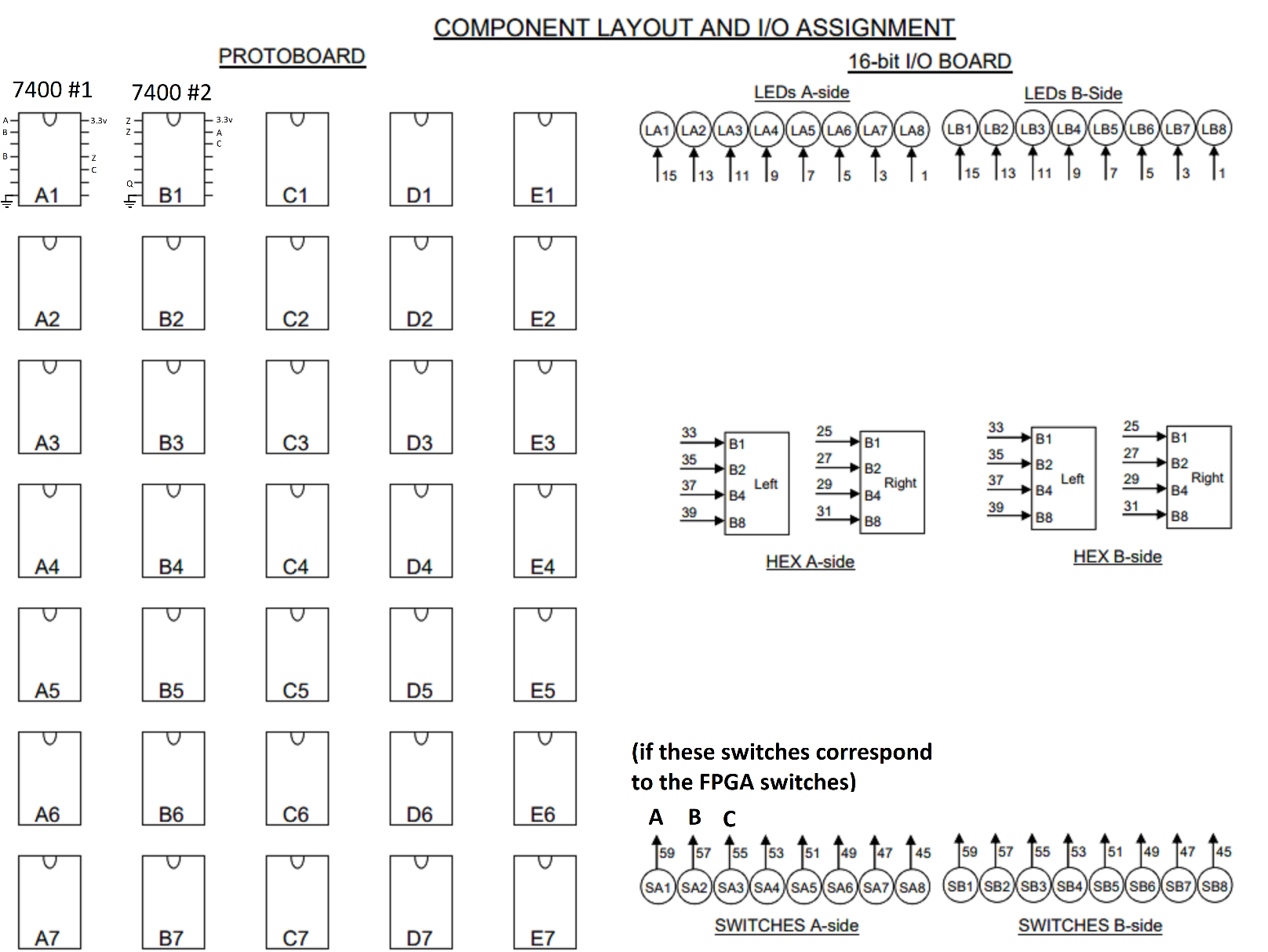




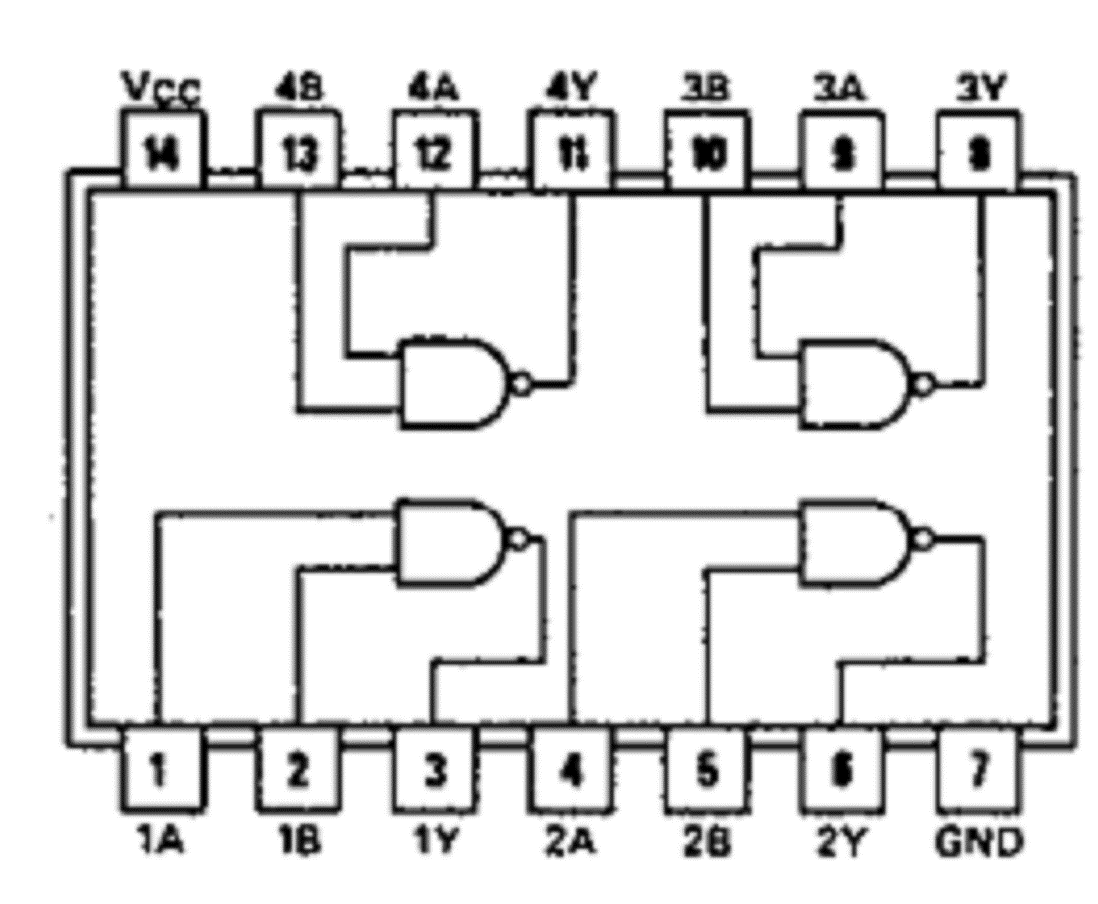
With this change, there is no visible difference when exploring all the variations of inputs and outputs between circuit A and the fixed circuit B. However, the oscilloscope reads a glitch free signal. Some noise is present due to switching but is not significant enough to affect the reliability of the logic diagram.



**Component Layout**



The pinnout of a SN7400 chip:



**Answers to Pre-Lab Questions**

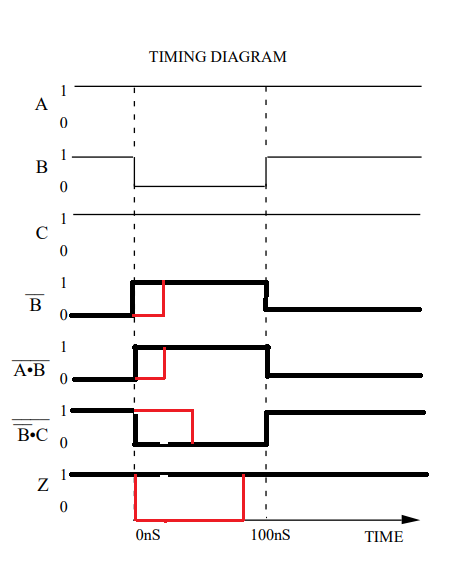
A static hazard may not be observed since it is only observed when switching between nonzero inputs. When you chain an odd number of inverters and/or adding a small capacitor to the output of the inverter produces a glitch because of the CMOS switch process. There is a momentary, but extremely short drop in voltage (connection to ground) when switching between nonzero inputs. This can affect the intended motions of logic within a circuit. The Designs for circuits part A and B are above in the report.

**Answers to Lab Questions**

The falling edge of input B is more likely to provide a glitch, since the negation of input B through the NAND gate has a delay which has not been registered by the other logic gates because their sequential delay is less because of the fewer amount of gates in sequence.

**Answers to Post-Lab Questions**

Red color accounts for the real delay of the gates. Theoretically, output Z should take 60ns max to stabilize on the falling edge of B since there are three logic gates of 20ns delays in sequence. It should take 40ns max for the rising edge of B to stabilize since there are only two logic gates for when B is switched on. The discrepancy between the two sequences of logic gates causes the glitch in the output Z since one line has two logic gates and the other has three. This causes one line to be ahead of the other, which is why a brief moment of low voltage is observed when the delay of the negation of B in the logic diagram has not been “realized” and turned on yet by the (B’C)’ line, but the (AB)’ is already off at this time.



2.) Explain how and why the debouncer circuit given in General Guide Figure 17 (GG.32) works. Specifically, what makes it behave like a switch and how the ill effect of mechanical contact bounces is eliminated?

Because a mechanical switch has initial bounces, pull-up resistors are used to bring up the logic level when it's not connected to ground in the SPDT switch, so that it doesn’t toggle when bouncing on and off the switch, unless otherwise intentionally connected in the other state of the switch.

what is the advantage of a larger noise immunity? Why is the last inverter observed rather than simply the first? Given a graph of output voltage (VOUT) vs. input GG.7 voltage (VIN) for an inverter, how would you calculate the noise immunity for the inverter?

The advantage of having larger noise immunity is for one reason simply upholding the intended proper output of logic. The last inverter is observed since it would have gone through the most variation of noise, as if it were the last one going through a game of telephone. The noise immunity would just be the greatest voltage the logical low can be at or lowest voltage the logical high can be at before switching to the other logic level. In this case, 2 and 0.8 volts respectively.

Irrespective of which polarity you choose for your LEDs, it is important that each LED has its own resistor. If we have two or more LEDs to monitor several signals, why is it bad practice to share resistors?

It is bad practice to share resistors because of power ratings, which may put a circuit at risk of breaking if not followed.

**Conclusions**

I have learned about the precautions one should take when designing logical circuits, as various glitches can occur, such as the static hazard in this lab. I also have taken note to utilize capacitors in finding issues that may not be perceivable at initial glance.